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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/537,124	06/02/2005	Sachin Aggarwal	492322028400	8384

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EXAMINER	
KEBEDE, BROOK	
ART UNIT	PAPER NUMBER
2823	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/537,124	AGGARWAL, SACHIN	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/2/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The preliminary amendment filed under 37 CFR 1.53(b) on June 2, 2005 is acknowledged and the amendment have been placed in the file.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 2-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites the limitation "A circuit layout configuration for matching two transistors, comprising: **a first transistor** comprising **eight first sub-transistors**; and a **second transistor** comprising **eight second sub-transistors**, wherein **the eight first sub-transistors** and the **eight second sub-transistors** are arranged in a four by four matrix, **the eight second sub-transistors** occupy eight diagonal positions of the four by four matrix, and **the eight first sub-transistors** occupy positions of the four by four matrix that are not the diagonal positions" in lines 1-7. However, is not clear the difference between the **"first"** and **"second"** transistor and **"the fist eight-sub transistors"** and **"the second eight-sub transistors"** for the following reasons:

The instant application claimed invention, as recited claim 8 above, is directed a matrix type "mesh-type" transistors layout for matching properties of MOSFETS. However, it is not clear form the claim what defines the "**first transistor**" and "**the second transistor**" and the correspondence "**the fist eight-sub transistors**" and "**the second eight-sub transistors.**"

Is it due to the type of transistors? Is it due to threshold adjustment of each of sub-transistor? Is it due to integration functionality of each sub-transistor? Is that due to the structure of the sub-transistor? Is any difference exist between "**first transistor**" and "**the second transistor**" similarly between "**the fist eight-sub transistors**" and "**the second eight-sub transistors.**" And etc.

Claim 7 also rejected for similar ground.

Since the claim is not clear in its meaning and the scope, for the above reasons, the aforementioned claim is indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 2-7 are also rejected as being directly or indirectly dependent of the rejected independent base claim.

Applicants' cooperation is requested in reviewing the claims structure to ensure proper claim construction and to correct any subsequently discovered instances of claim language noncompliance. See *Morton International Inc.*, 28USPQ2d 1190, 1195 (CAFC, 1993).

In light of the rejection 35 U.S.C. § 112 second Paragraph that set forth herein above, the following 35 U.S.C. 102 rejection is based on prior art which reads on the interpretation the claim language of the instant application as best as understood by the Examiner.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 2-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Ho (US 5,644,517).

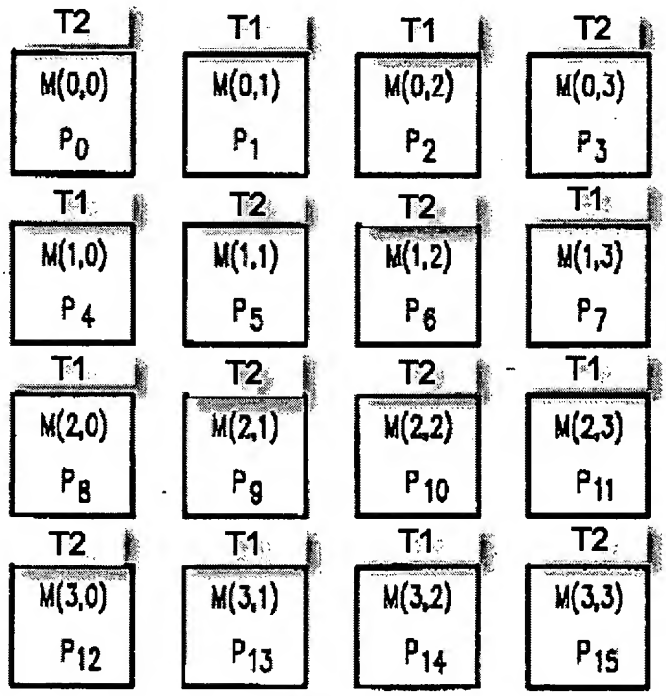

FIG. 2B

As shown Fig. 2B, Ho discloses mesh configuration of (i.e., 4 X 4 matrix circuit layout) circuit switch layout for concurrently performing a transportation of all data blocks on all processors including sub-mesh (i.e., sub-transistors). T1 = first transistor T2 second transistor and [M(0,0), M(1,1), M(2,2), M(3,3), M(0,3), M(1,2), M(2,1), M(0,3)]

are equivalent to the sub-transistors of the second transistor (T2), and [M(0,1), M(0,2), M(1,0), M(1,3), M(2,0), M(2,3), M(3,1), M(2,2)] are equivalent to the sub-transistors of the first transistor (T1).

Re claim 8, as shown in Fig. 2B, Ho discloses a circuit layout configuration for matching two transistors, comprising: a first transistor (T1) comprising eight first sub-transistors (i.e., [M(0,1), M(0,2), M(1,0), M(1,3), M(2,0), M(2,3), M(3,1), M(2,2)]); and a second transistor (T2) comprising eight second sub-transistors (i.e., [M(0,0), M(1,1), M(2,2), M(3,3), M(0,3), M(1,2), M(2,1), M(0,3)]), wherein the eight first sub-transistors (i.e., [M(0,1), M(0,2), M(1,0), M(1,3), M(2,0), M(2,3), M(3,1), M(2,2)]) and the eight second sub-transistors i.e., [M(0,0), M(1,1), M(2,2), M(3,3), M(0,3), M(1,2), M(2,1), M(0,3)]) are arranged in a four by four matrix, the eight second sub-transistors (i.e., [M(0,0), M(1,1), M(2,2), M(3,3), M(0,3), M(1,2), M(2,1), M(0,3)]) occupy eight diagonal positions of the four by four matrix, and the eight first sub-transistors (i.e., [M(0,1), M(0,2), M(1,0), M(1,3), M(2,0), M(2,3), M(3,1), M(2,2)])occupy positions of the four by four matrix that are not the diagonal positions (see Figs. 2A – 5 and related text Col. 2, line 1 through Col. 11, line 39).

Re claim 7, as applied to claim 8 above, Ho discloses all the claimed limitations including wherein the first transistor comprises eight additional first sub-transistors (see Figs. 4A-4C, the second transistor comprises eight additional second sub-transistors, and the eight additional first sub-transistors and the eight additional second sub-transistors are arranged so as to be symmetrical with the eight first sub-transistors and the eight second sub-transistors with respect to a line of symmetry (see Figs. 2A – 5 and related text Col. 2, line 1 through Col. 11, line 39).

Allowable Subject Matter

7. Claims 2-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 2-6 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Ogawa et al. (US 4,121,197), Oh et al. (US 5,959,928) and Fujino et al. (US 6,404,695) also disclose similar inventive subject matter.

Correspondence

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Brook Kebede

Brook Kebede
Primary Examiner
Art Unit 2823

BK
February 28, 2007